

HIGH-SPEED LOOKUP TABLE CIRCUITS AND METHODS FOR PROGRAMMABLE
LOGIC DEVICESABSTRACT

A lookup table (LUT) circuit comprises a multiplexer circuit having two modes. In a first mode, the multiplexer circuit functions as a standard multiplexer. In a second mode, the multiplexer circuit selects two or more stored values, where the two or more stored values have the same logical value. Thus, in the second mode the delay through the multiplexer circuit is reduced. In a PLD embodiment, two select terminals of the multiplexer are coupled to two different signal lines. When both signal lines are used, the multiplexer circuit is placed into the first mode. When only one of the signal lines is used, the multiplexer circuit is placed into the second mode, a value on the unused signal line is ignored, and two stored values are provided to the output terminal. Thus, the multiplexer circuit has a reduced path delay when one of the two signal lines is unused.